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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,455	09/18/2003	Keenan W. Franz	AUS920000709US2 (9000/93)	4359

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EXAMINER	
PEIKARI, BEHZAD	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,455	FRANZ ET AL.	
	Examiner	Art Unit	
	B. James Peikari	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-24,28-30 and 33-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33-35 and 37-40* is/are allowed.

6)☒ Claim(s) *21-24,28 and 36* is/are rejected.

7)☒ Claim(s) *29,30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. This application now includes the necessary reference to the prior application, due to the amendment filed on May 20, 2005.

Drawings

2. The previous objection to the drawings is withdrawn due to the amendment filed on April 1, 2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 21-24, 28 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrell et al., U.S. 5,014,195.

Farrell et al. teach the invention, including a microprocessor (*CPU 12, see section A below*) including a controller (*note cache controller 24*) and a multiplexor (*note select logic 38, which performs multiplexing functions*), a method of operating the microprocessor for supporting multiple cache configurations, the method comprising:

operating the controller to generate a first set of at least two address bit signals (*column 2, lines 63-66*) indicative of a first cache configuration (*note that the scope of the claimed "configuration" may include total size, logical partitioning, physical partitions, set associativity, etc.*) among the multiple cache configurations (*note that the address bits help determine, among other things, how many of and what portion of memories 26 need to be enabled and accessed, as well as the associativity of the cache, note column 5, lines 13-43*);

operating the controller to generate second set of at least two address bit signals indicative of a second cache configuration among the multiple cache configurations (*note that the table in column 7 describes a first cache configuration determined by at least two address bits, a second cache configuration determined by at least two other address bits, as well as a plurality of subsequent configurations determined by different combinations of bits*); and

operating the multiplexor to selectively communicate either the first set of at least two address bit signals or the second set of at least two address bit signals (*note that the address bits described in table 7 are included in the operation of the multiplexing provided by the select logic 38, note column 7, lines 15-17*) to a first memory device (*e.g., a first of cache memories 26*) and a second memory device (*e.g., any other cache memory 26*),

wherein a communication of the first set of at least two address bit signals to the first memory device and the second memory device is an indication of a selection of the first cache configuration during a boot of the microprocessor (*see section B below*), and

wherein a communication of the second set of at least two address bit signals to the first memory device and the second memory device is an indication of a selection of the second cache configuration during the boot of the microprocessor (*see section B below*).

Also, because the Farrell et al. reference is based on semiconductor technology, all of the elements have pins and all signals sent between one element and another must pass through pins.

With regard to the microprocessor *including* the controller and the multiplexor, this was not taught by Farrell et al., whose relevant controller and multiplexor was outside of the microprocessor 12, but still within the data processing system 12. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the cache device 22, or even just the

cache controller 24 (which contained the multiplexor 38) into the microprocessor 12, since to have the controller share the chip (1) might have reduced distance delays, thus providing faster communication, (2) might have reduced signal loss associated with longer lines, thus providing more efficient power consumption, (3) might have reduced the number of errors in transmission associated with longer lines and (4) to make integral was not generally given patentable weight, note *In re Larson*, 144 USPQ 347 (CCPA 1965), which was later upheld for electrical circuitry by *In re Tomoyuki Kohno*, 157 USPQ 275 (CCPA 1968).

Response to Amendment

6. With regard to applicant's remarks submitted with the amendment filed on May 20, 2005, these remarks have been carefully considered by the examiner with the following results:

(A) With regard to applicant's comments on page 10 of the remarks, these rely on the statement 'the cache configuration signals 28 are sent from the select logic 38 to a cache controller signal, rather than to the pins". However, this interpretation is incorrect. A signal can never be sent to a signal. A signal must be sent to a device. In this case, because the Farrell et al. reference is based on semiconductor technology, all of the elements have pins and all signals sent between one element and another must pass through pins. Consequently, the rejections above have been maintained.

(B) With regard to applicant's comments in the first paragraph of page 11 of the remarks, these are deemed convincing. See Sections 7 and 8 below.

Allowable Subject Matter

7. Claims 33-35 and 37-40 are allowed.

8. Claims 29 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (571) 272-

4185. The examiner is generally available between 7:00 am and 7:30 pm, EST, Monday through Wednesday, and between 5:30 am and 4:00 pm on Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (571) 272-4182.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center at 866-217-9197 (toll-free).

B. James Peikari
Primary Examiner
Art Unit 2189
7/11/05